REMARKS

The Office Action dated November 12, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1 and 11 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-20 are pending in the present application and are respectfully submitted for consideration.

Claims 1-20 Recite Patentable Subject Matter

Claims 1-2 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. (KR2002080953A, "Lee"). Applicants respectfully traverse the rejection and submit that the prior art fails to disclose or suggest each and every element recited in claims 1-2 of the present application.

In response to this rejection, Applicants have reviewed the teaching of Lee and found several reasons that the teaching of Lee is insufficient to render the claim unpatentable. In the teaching of Lee, a method for manufacturing semiconductor device is provided. In the illustrated drawing and abstract of Lee, the semiconductor device has LDD region 112 formed in the silicon substrate 101 and a silicon epitaxial layer formed on the entire surface of the resultant structure. However, the silicon epitaxial layer is deposited to form an elevated source and drain structure which is contrary to the claimed invention. The silicon epitaxial layer on the gate electrode 108 must be removed and an ion implantation process is then performed to complete the elevated

source and drain structure, which is also contrary to the teaching of the claimed invention. It is quite clearly that the teaching of Lee actually fails to teach every element of the claimed invention and one with ordinary skill in the art would not anticipate the claimed invention by the teaching of Lee.

Therefore, Applicants submit that Lee fails to disclose or suggest at least a method of surface pretreatment before selective epitaxial growth process, having among other features, the steps of providing a semiconductor substrate having metal-oxide-semiconductor devices each comprising a gate electrode, a source region and a drain region, and performing a selective epitaxial growth process to form a semiconductor layer on said gate electrode, said source and drain regions for a salicide process. As such, it is submitted that claim 1 is allowable.

As claim 2 depends from claim 1, Applicants submit that claim 2 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Claims 1-3 were rejected under 35 U.S.C. § 102(e) as being anticipated by anticipated by Murthy et al. (U.S. Patent No. 6,541,343, "Murthy"). Applicants respectfully traverse the rejection and submit that the prior art fails to disclose or suggest each and every element recited in claims 1-3 of the present application.

In response to this rejection, Applicants have reviewed the teaching of Murthy and found several reasons that the teaching of Murthy is insufficient to render the claim unpatentable. In the teaching of Murthy, a method of making field effect transistor

structure with partially isolated source/drain junctions is provided. In the illustrated drawings and specification of Murthy, the field effect transistor structure has source/drain region 216/408 formed in the semiconductor substrate 201 and a single crystal silicon epitaxial layer formed in the recess 212 of the semiconductor substrate 201. However, the silicon epitaxial layer is deposited to form a source and drain structure, which is completely contrary to the claimed invention. The silicon epitaxial layer is not formed on the gate electrode 202 and an ion implantation process is then performed to complete the source and drain structure, which is also contrary to the teaching of the claimed invention. It is quite clearly that the teaching of Murthy actually fails to teach every element of the claimed invention and one with ordinary skill in the art would not anticipate the claimed invention by the teaching of Murthy.

Therefore, Applicants submit that Murthy fails to disclose or suggest at least a method of surface pretreatment before selective epitaxial growth process, having among other features, the steps of providing a semiconductor substrate having metal-oxide-semiconductor devices each comprising a gate electrode, a source region and a drain region, and performing a selective epitaxial growth process to form a semiconductor layer on said gate electrode, said source and drain regions for a salicide process. As such, it is submitted that claim 1 is allowable with respect to Murthy.

As claims 2 and 3 depend from claim 1, Applicants submit that each of claims 2 and 3 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to independent claim 1, as well as for the additional subject matter recited therein.

Claims 4, 6 and 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, and claims 4-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Murthy. Applicants respectfully traverse these rejections and submit that the prior art fails to disclose or suggest each and every element recited in claims 4-9 of the present application.

Applicants respectfully submit that it would not be obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee and/or Murthy to disclose every element of the claimed invention. According to MPEP § 2143, Basic Requirements of a Prima Facie Case of Obviousness [R-1], to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must each or suggest al the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). That is, according to the last basic criteria of MPEP § 2143, the teachings of these references actually fail to teach or suggest all the claim limitations. Therefore, the

teachings of citations are actually insufficient to render the claimed invention unpatentable. Therefore, claims 4-9 are also allowable.

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Kodama (U.S. Patent No. 5,953,605, "Kodama"), and claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Murthy in view of Kodama. Applicants respectfully traverse these rejections and submit that the prior art fails to disclose or suggest each and every element recited in claim 10 of the present application.

Applicants submit that Kodama fails to cure the deficient elements of the claimed invention that exist in Lee, and similarly fails to cure the deficient elements of the claimed invention that exist in Murthy. Thus, the combination of Lee and Kodama, and the combination of Murthy and Kodama actually do not meet MPEP § 2143, Basic Requirements of a Prima Facie Case of Obviousness [R-1] so that the combination of Lee and Kodama is not sufficient to render the claimed invention prima facie obvious.

Furthermore, as claim 10 depends from claim 1, Applicants submit that claim 10 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to independent claim 1, as well as for the additional subject matter recited therein.

Claims 11-17 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu (U.S. Patent No. 6,190,977, "Wu") in view of Murthy. Applicants respectfully traverse these rejections and submit that the prior art fails to disclose or

suggest each and every element recited in claims 11-17 and 19-20 of the present application.

Wu merely discloses a method of forming MOSFET with an elevated source/drain. In the teaching of Wu, a gate insulator layer is formed over the semiconductor substrate and a first silicon layer is then formed over the gate insulator layer. A first dielectric layer is formed over the first silicon layer. A gate region is defined by removing a portion of the gate insulator layer, of the first silicon layer, and of the first dielectric layer. A doping step using low energy implantation or plasma immersion is carried out to dope the substrate to form an extended source/drain junction in the substrate under a region uncovered by the gate region. An undoped spacer structure is formed on sidewalls of the date region and a second silicon layer is formed on the semiconductor substrate. The first dielectric layer is then removed and another doping step is performed to dope the first silicon layer and the second silicon layer. A series of process is then performed to form a metal silicide layer on the first silicon layer and the second silicon layer and also to diffuse and activate the doped dopants.

In response to this rejection, Applicants have found several reasons that the teaching of Wu is insufficient to render the claim unpatentable. In the teaching of Wu, the semiconductor device has extended source/drain region 30 formed in the semiconductor substrate 10 and a second silicon layer epitaxially formed on the surface of the extended source/drain 30 but not on the surface of the first silicon layer 16/gate electrode. However, the second silicon layer is epitaxially deposited to form an elevated source and drain structure and is not formed on the surface of the first silicon layer must

be implanted and heated for diffusion to complete the elevated source and drain structure which is also contrary to the teaching of the claimed invention. Moreover, the elevated source and drain structure is completed after the second silicon layer is epitaxially formed on the surface of the extended source/drain region 3 excluding on the surface of the first silicon layer 16/gate electrode which is contrary to the claimed invention.

Therefore, Applicants submit that Wu fails to disclose or suggest at least a method of forming a semiconductor device using selective epitaxial growth comprising, among other features, the steps of forming a source/drain region with said second conductivity beside said lightly doped drain region in said semiconductor substrate, performing a selective epitaxial growth process to form a semiconductor layer on said gate electrode, said source and drain regions, and performing a salicide process to form a silicide layer on said gate electrode, said source and drain regions.

It is submitted that Murthy does not disclose the deficient elements of the claimed invention that exist in Wu. Therefore, the combination of Wu and Murthy actually does not meet MPEP § 2143, Basic Requirements of a Prima Facie Case of Obviousness [R-1] so that the combination of Wu and Murthy is not sufficient to render the claimed invention prima facie obvious, and thus claim 11 is allowable.

As claims 12-17, 19 and 20 depend from claim 11, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well

as for the additional subject matter recited therein. As such, claims 12-17, 19 and 20 are also allowable.

Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu and Murthy and further in view of Kodama. Applicants respectfully traverse this rejection and submit that the prior art fails to disclose or suggest each and every element recited in claim 18 of the present application.

Murthy and Kodama are discussed above. Applicants submit that Kodama also does not disclose the elements of the claimed invention that are missing from Wu and Murthy. The combination of Wu, Murthy and Kodama actually does not meet MPEP § 2143, Basic Requirements of a Prima Facie Case of Obviousness [R-1] so that the combination of Wu, Murthy and Kodama is not sufficient to render the claimed invention prima facie obvious. Thus, claim 18 is allowable.

Furthermore, as claim 18 depends from claim 11, Applicants submit that claim 18 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to independent claim 11, as well as for the additional subject matter recited therein. As such, claim 18 is also allowable.

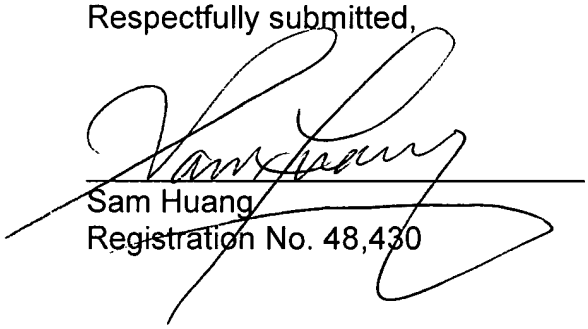
Conclusion

In view of the above, Applicants respectfully submit that each of claims 1-20 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-20 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 025796-00013.

Respectfully submitted,



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